

We claim:

- 1    1.    An apparatus comprising:  
2            an execution core;  
3            a scan chain to transfer data to one or more nodes of the execution core; and  
4            a reset module to provide a bit pattern to the scan chain, responsive to a reset  
5            signal.
- 1    2.    The apparatus of claim 1, wherein the execution core includes first and second execution  
2            cores to be operated in FRC mode, and wherein the scan chain includes first and second scan  
3            chains corresponding to the first and second execution cores, respectively.
- 1    3.    The apparatus of claim 2, wherein the reset module provides an identical bit pattern to the  
2            first and second scan chains, responsive to the reset signal.
- 1    4.    The apparatus of claim 3, wherein the reset module drives the first and second scan  
2            chains in parallel.
- 1    5.    The apparatus of claim 1, wherein the reset module further comprises:  
2            a clock mux to provide a first or second clock signal to the scan chain, responsive  
3            to a reset signal; and

4 a pattern generator to store the bit pattern and to provide the bit patter to the scan  
5 chain, responsive to the reset signal.

1 6. The apparatus of claim 5, wherein the reset module further comprises a mode selector to  
2 assert a signal to the clock mux and the pattern generator, responsive to assertion of the reset  
3 signal.

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3                   applying the bit pattern to a data line of the scan chain.

1    11.    The method of claim 9, further comprising propagating the reset signal to selected nodes  
2    of the processor through a reset tree.

1    12.    The processor of claim 11, further comprising executing a reset code module to place  
2    additional nodes of the processor into specified states.

1    13.    The method of claim 9 wherein the processor includes multiple execution cores to  
2    operate in FRC mode and wherein applying the bit pattern to the scan chain comprises applying  
3    the bit pattern to a corresponding scan chain in each of the execution cores.

1    14.    The method of claim 11, wherein applying the bit pattern to a corresponding scan chain  
2    in each execution core comprises applying the bit pattern in parallel to the corresponding scan  
3    chains.

1    15.    The method of claim 9, further comprising detecting an operating mode for the processor.

1    16.    The method of claim 15, wherein detecting the operating mode comprises determining if  
2    the operating mode is a high performance mode or a high reliability mode, and applying a bit

3 pattern to the scan chain comprises applying a bit pattern to the scan chain if the determined  
4 mode is the high reliability mode.

1 17. A system comprising:

2 first and second execution cores to be operated in an FRC mode, responsive to a  
3 mode bit, each of the execution cores including a scan chain to transfer data to a first set  
4 of nodes of the execution core;

5 an FRC checker to be activated in FRC mode to compare data from the first and  
6 second execution cores; and

7 a reset module to apply a bit pattern to the scan chains of the first and second  
8 execution cores, responsive to a reset event in the system.

1 18. The system of claim 17, wherein the reset module includes a pattern generator to drive  
2 the bit pattern on data lines of the scan chains of the first and second execution cores responsive  
3 to a scan clock.

1 19. The system of claim 18, further comprising a reset tree, the reset tree including electrical  
2 connections to a second set of nodes to drive the second set of nodes to specified states  
3 responsive to the reset event.

1 20. The system of claim 18, further comprising a storage device to store a reset code module,  
2 the reset code module to be executed by the first and second execution cores to drive a third set  
3 of nodes to specified states, responsive to the reset event.

1 21. The system of claim 20, wherein first, second and third sets of nodes are mutually  
2 exclusive.

1 22. An apparatus comprising:

2 an execution core including a set of voltage nodes coupled through data and clock  
3 lines;

4 a reset module to drive a data signal and a clock signal to the set of voltage nodes,  
5 responsive to occurrence of a reset event, the data signal to place the voltage nodes of the  
6 set in specified logic states.

1 23. The apparatus of claim 22, wherein the execution core comprises first and second  
2 execution cores, each having a set of voltage nodes coupled through clock and data lines, the first  
3 and second execution cores to be operated in an FRC mode.

1 24. The apparatus of claim 23, wherein the data signal driven by the reset module is a bit  
2 pattern that places the set of voltage nodes of the first and second execution cores in the specified  
3 logic states.

1 25. The apparatus of claim 24, wherein the reset module drives the set of voltage nodes of the  
2 first and second execution cores in parallel.

1 26. The apparatus of claim 22, wherein the execution core comprises first and second  
2 execution cores, each having a set of voltage nodes, the first and second execution cores to be  
3 operated in an FRC mode, responsive to a mode bit being in a first state.

1 27. The apparatus of claim 26, wherein the reset module is disabled and the execution cores  
2 are operated in a non-FRC mode, responsive to the mode bit being in a second state.

1 28. The apparatus of claim 22, further comprising a reset tree to drive a second set of voltage  
2 nodes of the apparatus to second logic states, responsive to occurrence of a reset event.

1 29. The apparatus of claim 28 further comprising a storage device to store a reset code  
2 module, the reset code module to be executed by the execution core to place a third set of voltage  
3 nodes in specified logic states, responsive to the reset event.

1 30. The apparatus of claim 29, wherein the reset module establishes specified logic states for  
2 the first set of voltage nodes before the reset code module is executed.